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1. Changed to async

library IEEE;  
use IEEE.STD\_LOGIC\_1164.ALL;  
use IEEE.STD\_LOGIC\_ARITH.ALL;  
use IEEE.STD\_LOGIC\_UNSIGNED.ALL;  
...  
 StateReg: PROCESS (Clk, Rst)  
 BEGIN  
 IF (Rst = '1') THEN  
 CurrentState <= S\_Off;  
 ELSIF (Clk = '1' AND Clk'EVENT) THEN  
 CurrentState <= NextState;  
 END IF;  
 END PROCESS StateReg;

...

1. Changed stuff

...  
CombLogic: PROCESS (CurrState, C1, C0)  
 BEGIN  
 CASE CurrState IS  
 WHEN S\_Off =>  
 IF (C1 = '0') THEN  
 NextState <= S\_Off;  
 ELSE  
 IF (C0 = '0') THEN  
 NextState <= S\_On1;  
 ELSE  
 NextState <= S\_On2;  
 END IF;  
 END IF;  
 WHEN S\_On1 =>  
 IF (Rst = '1') THEN  
  NextState <= S\_Off;  
 ELSE  
 IF (C0 = '0) THEN  
 NextState <= S\_On1;  
 ELSE  
 NextState <= S\_On2  
 END IF;  
 END IF;  
 WHEN S\_On2 =>  
 IF (Rst = '1') THEN  
  NextState <= S\_Off;  
 ELSE  
 IF (C1 = '0) THEN  
 NextState <= S\_On2;  
 ELSE  
 NextState <= S\_On1  
 END IF;  
 END IF;  
 END CASE;  
END PROCESS CombLogic;  
  
StateReg: PROCESS (Clk, Rst)  
BEGIN  
 IF (Clk = '1' AND Clk'EVENT) THEN  
 CurrState <= NextState;  
 END IF;  
END PROCESS StateReg;  
...